What is Claimed is:

[c1] A method of generating a clock signal on an integrated circuit (IC), the method comprising the steps of:

generating a differential sinusoidal signal pair; and

generating a clock signal from the differential pair for the IC.

[c2] The method of claim 1, wherein the step of generating a clock signal includes supplying the differential pair to a differential amplifier.

[c3] The method of claim 1, wherein the differential pair has a peak to peak differential of not more than about 150 mV.

[c4] The method of claim 3, wherein the differential pair has a peak to peak differential of substantially 100 mV.

[c5] The method of claim 1, further comprising routing the differential pair to a plurality of clock receivers.

[c6] The method of claim 5, wherein the differential pair is routed in adjacent tracks.

[c7] The method of claim 1, further comprising applying clock gating at the clock receivers.

[c8] A method of driving a clock tree on an integrated circuit (IC), the method comprising the step of:

providing an IC having a clock tree; and

distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree.

[c9] The method of claim 8, wherein the differential pair has a peak to peak differential of not more than about 150 mV.

[c10] The method of claim 9, wherein the differential pair has a peak to peak differential of substantially 100 mV.

[c11] The method of claim 8, further comprising converting the differential sinusoidal signal pair to a local clock signal by using a differential amplifier.

[c12] The method of claim 11 wherein the local clock signal has an amplitude substantially

equal to a power supply voltage, and the differential sinusoidal signal pair has a peak to peak differential that is substantially less than the amplitude of the local clock signal.

[c13] A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal pair;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals.

[c14] The clock circuit of claim 13, wherein the local clock signals have an amplitude substantially equal to a power supply voltage, and the differential sinusoidal signal pair has a peak to peak differential that is substantially less than the amplitude of the local clock signals.

[c15] The clock circuit of claim 14, wherein the peak to peak differential of the differential sinusoidal signal pair is less than half the amplitude of the local clock signals.

[c16] The clock circuit of claim 15, wherein the peak to peak differential of the differential sinusoidal signal pair is less than one-fifth the amplitude of the local clock signals.

[c17] The clock circuit of claim 16, wherein the peak to peak differential of the differential sinusoidal signal pair is less than one-tenth the amplitude of the local clock signals.

[c18] The clock circuit of claim 13, wherein the differential pair has a peak to peak differential of not more than about 150 mV.

[c19] The clock circuit of claim 18, wherein the differential pair has a peak to peak differential of substantially 100 mV.

[c20] The clock circuit of claim 13, wherein each of the clock receiver circuits includes a differential amplifier.

[c21] The clock circuit of claim 13 wherein the distribution circuit includes means for tuning a frequency response of the distribution circuit.

[c22] Apparatus for generating and distributing a clock signal, comprising:

means for generating a differential sinusoidal signal pair;

means for distributing the generated differential sinusoidal signal pair; and means for receiving the distributed differential sinusoidal signal pair and converting the received differential sinusoidal pair into a local clock signal.

[c23] The apparatus of claim 22, further comprising a clock splitter for splitting the local clock signal.

[c24] The apparatus of claim 22, wherein the local clock signal has an amplitude substantially equal to a power supply voltage, and the differential sinusoidal signal pair has a peak to peak differential that is substantially less than the amplitude of the local clock signal.

[c25] The apparatus of claim 24, wherein the peak to peak differential of the differential sinusoidal signal pair is less than half the amplitude of the local clock signal.

[c26] The apparatus of claim 25, wherein the peak to peak differential of the differential sinusoidal signal pair is less than one-fifth the amplitude of the local clock signal.

[c27] The apparatus of claim 26, wherein the peak to peak differential of the differential sinusoidal signal pair is less than one-tenth the amplitude of the local clock signal.

[c28] The apparatus of claim 22, wherein the differential pair has a peak to peak differential of not more than about 150 mV.

[c29] The apparatus of claim 28, wherein the differential pair has a peak to peak differential of substantially 100 mV.

[c30] The apparatus of claim 22, wherein the means for receiving and converting includes a differential amplifier.